

What are Memristor, Memcapacitor, and Meminductor?

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Abstract—Memristor, memcapacitor, and meminductor are new fundamental circuit elements, whose properties depend on the history of devices. This paper presents the physical analysis of these memory devices. Three simple examples are given for the memristor, memcapacitor, and meminductor, and are then generalized to reveal their general physical origin. It is found that the memristance, memcapacitance, and meminductance are caused by different combinations of nonlinear electric responses. The mathematical expressions for the currents through any voltage-driven memristor, memcapacitor, and meminductor are given, and the corresponding expressions for the memristance, memcapacitance, and meminductance are derived. Moreover, a method to determine the charge–flux relationship of a memristor is proposed.

Index Terms—Circuit element, memory device, memristor, nonlinear electric response.

I. INTRODUCTION

IN 1971, Chua envisioned the missing fourth circuit element, the memristor, in addition to resistor, capacitor, and inductor [3]. More detailed discussions on a broad generalization of memristors as memristive systems were published in 1976 [4]. The memristor is a two-terminal nonlinear electric element. In 2008, 37 years after it was proposed, Chua’s missing memristor was finally discovered by a team of researchers at Hewlett-Packard [5], [6], and it was based on a thin film of titanium dioxide. Memristor has become an important subject of study, and several research activities have flourished since then [7]–[26]. For instance, the first hybrid memristor/CMOS device was built for future data storage and neuromorphic applications [10].

The memristor was conceptualized by analyzing the relationships among current i , charge q , voltage v , and flux ϕ . There are six different mathematical relations of connecting pairs of these four variables. Charge q and flux ϕ are the time integral of the current i and the voltage v , respectively, and the remaining four relationships should define the four fundamental circuit elements: the resistor, the capacitor, the inductor, and the missing fourth element, i.e., the memristor. The memristor was the missing link between flux ϕ and charge q . The memristance

$M(q)$, can be defined as the derivative of the flux ϕ with respect to the charge q

$$M(q) = \frac{d\phi(q)}{dq}. \quad (1)$$

Recently, the concept of the memristor was extended to the memcapacitor and meminductor by Chua [1], [2], which are defined as

$$C(\phi) = \frac{d\sigma(\phi)}{d\phi} \quad (2)$$

$$L(q) = \frac{d\rho(q)}{dq} \quad (3)$$

where $\sigma(\phi)$ is a differentiable function of ϕ , and $\rho(q)$ is a differentiable function of q , with $\sigma = \int_{-\infty}^t \phi(\tau) d\tau$ and $\rho = \int_{-\infty}^t q(\tau) d\tau$, respectively.

Seen clearly from the above analysis, the theories on the memristor, memcapacitor, and meminductor are so far phenomenological. It would be interesting to understand the physical mechanisms of these new circuit elements. In this paper, we only focus on the ideal memristor, memcapacitor, and meminductor. Prior to the discussion on the general mechanism of memristor, memcapacitor, and meminductor, we examine three specific examples: a memristor, a memcapacitor, and a meminductor. The three devices are all driven by a sinusoidal applied voltage, i.e.,

$$v(t) = A \sin \omega t \quad (4)$$

and the corresponding flux is expressed as

$$\phi(t) = \int_0^t A \sin \omega \tau d\tau = \frac{A}{\omega} (1 - \cos \omega t) \quad (5)$$

whose value is confined between 0 and $2A/\omega$. The initial conditions of charge $q(0) = \int_{-\infty}^0 i(\tau) d\tau$ and flux $\phi(0) = \int_{-\infty}^0 v(\tau) d\tau$ are also assumed zero in the following discussions.

II. THREE MATHEMATICAL EXAMPLES

A. Memristor

Assume a current through a system that can be described as follows:

$$i(t) = \sin \omega t + \frac{1}{5} \sin 2\omega t + \frac{1}{5} \sin 3\omega t. \quad (6)$$

Note that all the components of the current are sinusoidal. Plotting the locus of $(i(t), v(t))$ in the $i-v$ plane, a hysteresis loop that is pinched at $(0, 0)$ is found, as shown in Fig. 1(a), which is an important characteristic of a memristor. To confirm that it is indeed a memristor, the $q-\phi$ curve should be single

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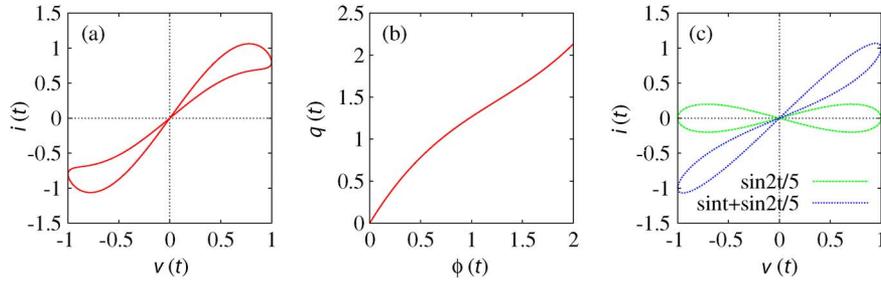


Fig. 1. (Color online) (a) $i-v$ curve of the memristor whose current is expressed in (6). (b) Single-valued relationship between $q(t)$ and $\phi(t)$. (c) Different $i-v$ loci with the green curve for the second term on the right-hand side (RHS) of (6) and the blue curve for the sum of the first and second terms on the RHS of (6). For simplicity, both parameters A and ω are set to 1.

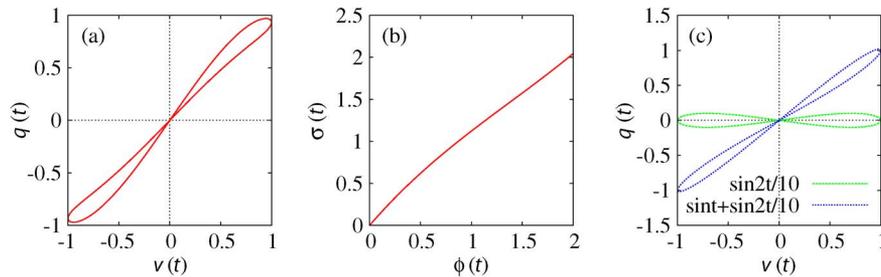


Fig. 2. (Color online) (a) $q-v$ curve of the memcapacitor. (b) Single-valued relationship between $\sigma(t)$ and $\phi(t)$. (c) Different loci with the green curve for the second term on the RHS of (10) and the blue curve for the sum of the first and second terms on the RHS of (10). For simplicity, both parameters A and ω are set to 1.

valued with respect to ϕ . With a simple transformation, $q(t)$ as a function of ϕ can be expressed as

$$q(\phi) = \frac{2}{A}\phi - \frac{\omega}{A^2}\phi^2 + \frac{4\omega^2}{15A^3}\phi^3 \quad (7)$$

and thus, q is indeed a single-valued function of ϕ , as confirmed in Fig. 1(b). The pinched hysteresis $i-v$ loop together with the single-valued $q-\phi$ curve indicate that such a system is a memristor. The corresponding memductance can be evaluated as

$$G(\phi) = \frac{dq}{d\phi} = \frac{2}{A} - \frac{2\omega}{A^2}\phi + \frac{4\omega^2}{5A^3}\phi^2. \quad (8)$$

B. Memcapacitor

There are many forms of the electric current through different memcapacitors. Let us examine one of these

$$i(t) = \cos \omega t + \frac{1}{5} \cos 2\omega t + \frac{1}{5} \cos 3\omega t \quad (9)$$

and note that the current components are cosinusoidal with three different frequencies. The corresponding charge is then obtained as

$$q(t) = \frac{1}{\omega} \sin \omega t + \frac{1}{10\omega} \sin 2\omega t + \frac{1}{15\omega} \sin 3\omega t. \quad (10)$$

A pinched hysteresis loop in the $q-v$ plane is indeed shown in Fig. 2(a), which is indicative of a memcapacitor. The single-valued function relationship can also be obtained between the time integration of charge q and the flux ϕ as follows:

$$\sigma(\phi) = \frac{21}{15A\omega}\phi - \frac{11}{30A^2}\phi^2 + \frac{4\omega}{45A^3}\phi^3 \quad (11)$$

where the initial condition $\sigma(0) = \int_{-\infty}^0 q(\tau) d\tau = 0$. The locus of $(\sigma(t), \phi(t))$ is shown in Fig. 2(b) and is confirmed as a single-valued curve with respect to ϕ . Therefore, the corre-

sponding device for (9) is indeed a memcapacitor, and its memcapacitance is evaluated as

$$C(\phi) = \frac{d\sigma}{d\phi} = \frac{21}{15A\omega} - \frac{11}{15A^2}\phi + \frac{4\omega}{15A^3}\phi^2. \quad (12)$$

C. Meminductor

Since we have examined two forms of current, let us now examine the following current:

$$i(t) = -\cos \omega t + \frac{1}{5} \sin 2\omega t + \frac{1}{5} \cos 3\omega t. \quad (13)$$

A pinched hysteresis loop can now be observed from the locus of $(i(t), \phi(t))$, as shown in Fig. 3(a). The relationship between $q(t)$ and $\rho(t) = \int_0^t \phi(\tau) d\tau$ (for simplicity, initial condition $\rho(0) = \int_{-\infty}^0 \phi(\tau) d\tau = 0$) is shown in Fig. 3(b), showing that q is a single-valued function of ρ . Therefore, the device that the current [as described in (13)] goes through is a meminductor. If an initial flux is chosen to be $\phi(0) = \int_{-\infty}^0 v(\tau) d\tau = -(A/\omega)$, the crossing point will be at origin, and the corresponding inverse meminductance is evaluated to be

$$L^{-1}(\rho) = \frac{dq}{d\rho} = \frac{4\omega}{5A} + \frac{2\omega^3}{5A^2}\rho + \frac{4\omega^5}{5A^3}\rho^2. \quad (14)$$

Before we proceed further, let us reflect on what we have learned from the analysis of the three examples given. We have seen that the current through a memristor is made of pure sinusoidal components, the current through a memcapacitor is of pure cosinusoidal, and the current through a meminductor is a hybrid of both sinusoidal and cosinusoidal components. The question is whether the given observation can be extended for the general memristor, memcapacitor, and meminductor. Note that we focus our discussion on ideal memristor, memcapacitor, and meminductor throughout this brief.

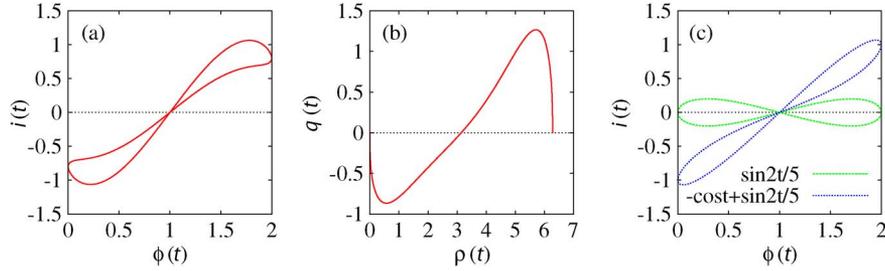


Fig. 3. (Color online) (a) i - ϕ curve of the meminductor. (b) Locus of $(q(t), \phi(t))$ that shows that q is a single-valued function of ϕ (t is set from 0 to 2π). (c) Different i - ϕ loci with the green curve for the second term on the RHS of (13) and the blue curve for the sum of the first and second terms on the RHS of (13). For simplicity, both parameters A and ω are set to 1.

III. GENERAL FORMALISM FOR MEMRISTOR, MEMCAPACITOR, AND MEMINDUCTOR

Now let us examine an arbitrary current driven by the sinusoidal applied voltage described in (4). The current can be expressed in term of the following Fourier series:

$$\begin{aligned} i(t) = & a_1 \cos \omega t + b_1 \sin \omega t + \sum_{k=1} a_{2k} \cos 2k\omega t \\ & + \sum_{k=1} b_{2k} \sin 2k\omega t + \sum_{k=1} a_{2k+1} \cos(2k+1)\omega t \\ & + \sum_{k=1} b_{2k+1} \sin(2k+1)\omega t. \end{aligned} \quad (15)$$

In fact, $b_1 \sin \omega t$ corresponds to a current through a conventional resistor with resistance equal to A/b_1 , and $a_1 \cos \omega t$ corresponds to a current through a conventional capacitor or inductor (depending on the sign of a_1) with capacitance or inductance that is equal to $a_1/\omega A$ or $-(A/\omega a_1)$, respectively. Both $b_1 \sin \omega t$ and $a_1 \cos \omega t$ are linear responses, and the rest are the nonlinear responses. We show in the following that different terms in (15) can be categorized into the memristor, memcapacitor, and meminductor.

A. Memristor

Selecting the second, fourth, and sixth terms on the RHS of (15), and summing them up, we have the following current expression:

$$i^R(t) = b_1 \sin \omega t + \sum_{k=1} b_{2k} \sin 2k\omega t + \sum_{k=1} b_{2k+1} \sin(2k+1)\omega t \quad (16)$$

which is a generalization of (6). We will show that i^R represents in fact the current through a memristor. The second term of (16) can be expressed as

$$\sum_{k=1} b_{2k} \sin 2k\omega t = \sum_{k=1} b_{2k} F_{2k}(v^*) \cos \omega t \quad (17)$$

where $v^* = v/A = \sin \omega t$, and

$$\begin{aligned} F_{2k}(v^*) = & C_{2k}^1 (1 - v^{*2})^{k-1} v^* + i^2 C_{2k}^3 (1 - v^{*2})^{k-2} v^{*3} \\ & + \dots + i^{2k-4} C_{2k}^{2k-3} (1 - v^{*2}) v^{*2k-3} \\ & + i^{2k-2} C_{2k}^{2k-1} v^{*2k-1} \end{aligned} \quad (18)$$

where $C_m^n = m!/[n!(m-n)!]$. The last term of (16) can be expressed in the same way. When v is 0, i.e., when

$\omega t = n\pi$ ($n = 0, 1, 2, \dots$), $i^R = 0$, and the slope of i - v curve at the origin $(0, 0)$ can be evaluated as

$$\frac{di^R}{dv} = \frac{di^R}{A dv^*} = \frac{1}{A} \left[b_1 + \sum_{k=1} b_{2k} 2k \cos \omega t + \sum_{k=1} b_{2k+1} (2k+1) \right]. \quad (19)$$

Since $\cos \omega t$ can be 1 or -1 at the origin, (19) is double valued as well. As a result, the locus of $(i^R(t), v(t))$ goes through $(0, 0)$ with two different slopes, which results in a hysteresis loop pinched at the origin $(0, 0)$, i.e., a characteristic of a memristor.

The first term on the RHS of (16) corresponds to the current contribution from a resistor with the resistance of A/b_1 , and the third term corresponds to the nonlinear resistance. The second term is responsible for the double-valued i^R at the same v and thus for the hysteresis loop. Equation (6) is a special case of (16). We plot separately the loci $(i(t), v(t))$ for the second term and the sum of first and second terms in Fig. 1(c). The green loop is for the second term only and note that it has negative resistance. Inclusion of the first term leads to a normal hysteresis loop of a memristor and elimination of the negative resistance. Further inclusion of the third term leads to more variation to the hysteresis loop. The higher order sinusoidal terms would result in further variation and even more pinched points along the hysteresis loop.

A further test for the memristor is that the charge q should be a single-valued function of ϕ . With some simple algebra, the charge $q^R(\phi)$ for the current (16) can be expressed as follows:

$$q^R(\phi) = \sum_{k=1}^N \frac{b_k [1 - T_k(1 - \frac{\omega}{A}\phi)]}{k\omega} \quad (20)$$

where T_k is the Chebyshev polynomials of the first kind [25], which confirms that the charge q^R is indeed a single-valued function of the flux ϕ (with $\phi \in [0, 2A/\omega]$). We conclude that (16) corresponds to the current through a memristor. The corresponding memductance is readily evaluated as

$$G^R(\phi) = \sum_{k=1}^N \frac{b_k}{A} U_{k-1} \left(1 - \frac{\omega}{A}\phi \right) \quad (21)$$

where U_k is the Chebyshev polynomials of the second kind.

B. Memcapacitor and Meminductor

Generalizing the current expression (9), we have the general expression for the current through a memcapacitor as follows:

$$i^C(t) = a_1 \cos \omega t + \sum_{k=1} a_{2k} \cos 2k\omega t + \sum_{k=1} a_{2k+1} \cos(2k+1)\omega t \quad (22)$$

and the corresponding charge can be expressed as

$$q^C(t) = \frac{a_1}{\omega} \sin \omega t + \sum_{k=1} \frac{a_k}{k\omega} \sin k\omega t. \quad (23)$$

When a_1 is positive, we have a conventional memcapacitor; otherwise, the memcapacitance is negative. Equation (23) leads to a hysteresis loop pinched at the origin (0, 0) in the $q-v$ plane. The corresponding memcapacitance can be described in the form of $\phi(t)$ as follows:

$$C(\phi) = \sum_{k=1} \frac{a_k}{Ak\omega} U_{k-1} \left(1 - \frac{\omega}{A} \phi\right). \quad (24)$$

Similarly, we may write down the general current form for any meminductor. Generalizing (13), we obtain the general expression for the current through a meminductor:

$$i^L(t) = a_1 \cos \omega t + \sum_{k=1} b_{2k} \sin 2k\omega t + \sum_{k=1} a_{2k+1} \cos(2k+1)\omega t. \quad (25)$$

It is easy to find that there is a pinched point at the (0, A/ω) in the $i^L - \phi$ plane. If one pick an initial flux at $t = 0$ as $\phi(0) = -(A/\omega)$, this hysteresis loop will be pinched at origin. It is straightforward to verify that $q^L(t)$ is a single-valued function of $\rho(t) = \int_0^t \phi(\tau) d\tau$. The inverse meminductance can be evaluated as a function of $\rho(t)$

$$\begin{aligned} L^{-1}(\rho) = & -\frac{a_1\omega}{A} + \frac{\omega}{A} \\ & \times \sum_{m=1} \left[b_{4m} U_{4m-1} \left(-\frac{\omega^2}{A} \rho\right) - b_{4m+2} U_{4m+1} \left(-\frac{\omega^2}{A} \rho\right) \right. \\ & - a_{4m+1} U_{4m} \left(-\frac{\omega^2}{A} \rho\right) \\ & \left. + a_{4m+3} U_{4m+2} \left(-\frac{\omega^2}{A} \rho\right) \right]. \quad (26) \end{aligned}$$

Although only voltage-driven cases are considered here, the responses of memristor, memcapacitor, and meminductor driven by current can be readily analyzed with the same method. If we apply a current source $i(t) = A \sin \omega t$ as an input to the meminductor, a voltage response containing only cosine terms will be observed. Then, the expression for flux $\phi(t)$ is identical to (23), consisting of only sine terms, and the expression for meminductance is the same as (24) (the only difference is that memcapacitance is replaced by meminductance). Similarly, if a memcapacitor is driven by a current source $i(t) = A \sin \omega t$, the voltage response will have an identical expression to the RHS of (25), and the inverse of memcapacitance can be solved as (26).

In fact, the way to prove the rule in [20] that pinched hysteresis loops of ideal memelements must be ‘‘self-crossing’’ is applicable to derivations of memristor, voltage-controlled memcapacitor, and current-controlled meminductor. However, it does not work for current-controlled memcapacitor and voltage-controlled meminductor since their output signals may not be parity functions of time, which is one of sufficient conditions to prove the rule. For example, the response current of meminductor described by (13) is neither odd nor even function of time. The expression of its inverse meminductance

cannot be derived from this rule directly. It is also noted that, according to the definitions of memristor, memcapacitor, and meminductor, the hysteresis loop must be pinched in the origin, for both ideal and generalized memory devices. It is easy to find that any other component beyond the combinations we have discovered may shift the crossing point away from the origin.

C. Measurement of $q-\phi$ Relationship of an Ideal Memristor

In laboratory, charge q and flux ϕ cannot be measured directly. Instead, we may measure the voltage and current. Applying a sinusoidal voltage, i.e., (4), we measure the output current and determine the Fourier coefficients $\{b_k\}$ in (16). Substituting $\{b_k\}$ and voltage information (amplitude A and frequency ω) into (20) and (21), the $q-\phi$ relationship as well as memductance can be evaluated. As a result, the response of this ideal memristor due to any bipolar voltage input within the range of flux inside $[0, 2A/\omega]$ can be predicted. Tuning the amplitude and frequency can vary the range of flux.

A device model is not useful unless it is predictable [5]. For an ideal memristor, its $q-\phi$ relationship should be unique and hold no matter how input signal varies, i.e., (20) and (21) should be independent of $\{b_k\}$, A , and ω . Equation (21) can be reorganized as

$$G^R(\phi) = \sum_{k=1}^N C_k \phi^{k-1} \quad (27)$$

where $\{C_k\}$ are parameters determined by intrinsic physics properties of the memristor and independent of the characteristics of the applied voltage. $\{C_k\}$ may be expressed in terms of the parameters $\{b_k\}$ or vice versa. For example, if $N = 3$, the relationship between $\{b_k\}$ and $\{C_k\}$ can be expressed as

$$\begin{aligned} b_3 &= C_3 \frac{A^3}{4\omega^2}, \quad b_2 = -C_2 \frac{A^2}{2\omega} - C_3 \frac{A^3}{\omega^2} \\ b_1 &= C_1 A + C_2 \frac{A^2}{\omega} + C_3 \frac{5A^3}{4\omega^2}. \quad (28) \end{aligned}$$

Here, C_1 , C_2 , and C_3 are the constants that are determined by intrinsic physical properties of the memristor and b_1 , b_2 , and b_3 depend explicitly on the amplitude and frequency of the applied voltage. As the frequency tends to infinity, b_2 and b_3 in (28) become zero, whereas b_1 approaches a constant; and consequently, the memductance $G^R(\phi)$ becomes a constant, which implies that the memristor reduces into a normal resistor when frequency is infinite, i.e., another one of the fingerprints of memristor [9].

D. General Bipolar Input

Instead of the simple sinusoidal applied voltage discussed so far, we generalize our study to a general case where the bias voltage is an arbitrary periodical signal without a dc term, i.e.,

$$v(t) = \sum_{k=1}^{N_1} A_k \sin k\omega t. \quad (29)$$

We prove in the following that the output current of an ideal memristor is of the same expression as (16).

According to (29), $v(t)$ is an odd function of time t , and the corresponding flux $\phi(t)$ is an even function of the time as it is the time integral of $v(t)$. As shown earlier, the memductance G of an ideal memristor is a function of ϕ . As a result, $G^R[\phi(t)]$ is an even function of time t . Therefore, the current $i^R(t) = G^R[\phi(t)]v(t)$ is an odd function of time t and can be expressed as

$$i^R(t) = \sum_{n=1}^N c_n \sin n\omega t. \quad (30)$$

The slope of the $i-v$ curve at the origin (0, 0) can be evaluated by

$$\frac{di^R}{dv} = \frac{di^R/dt}{dv/dt} = \frac{d \sum_{n=1}^N c_n \sin n\omega t / dt}{d \sum_{k=1}^N A_k \sin k\omega t / dt} = \frac{\sum_{n=1}^N n c_n \cos n\omega t}{\sum_{k=1}^N k A_k \cos k\omega t}. \quad (31)$$

By definition, the bipolar voltage goes to 0 at $\omega t = m\pi$ ($m = 0, 1, 2, \dots$) with the corresponding $\cos[2l\omega t] = 1$ and $\cos[(2l+1)\omega t] = \pm 1$, $l = 0, 1, 2, \dots$. Therefore, the slope of $i-v$ curve at the origin (0, 0) is double valued as

$$\frac{di^R}{dv} = \frac{\sum_{n=1}^N 2n c_{2n} \pm \sum_{n=1}^N (2n+1) c_{2n+1}}{\sum_{k=1}^N 2k A_{2k} \pm \sum_{k=1}^N (2k+1) A_{2k+1}} \quad (32)$$

which leads to a pinched hysteresis loop. The two slopes is degenerate only if

$$\sum_{n=1}^N 2n c_{2n} \cdot \sum_{k=1}^N (2k+1) A_{2k+1} = \sum_{n=1}^N (2n+1) c_{2n+1} \cdot \sum_{k=1}^N 2k A_{2k}. \quad (33)$$

The flux ϕ and charge q can be evaluated from (29) and (30) as $\phi(t) = \sum_{k=1}^N (b_k/k\omega)(1 - \cos k\omega t)$ and $q(t) = \sum_{n=1}^N (c_n/n\omega)(1 - \cos n\omega t)$. For simplicity, initial conditions $\phi(0) = \int_{-\infty}^0 v(\tau) d\tau$ and $q(0) = \int_{-\infty}^0 i(\tau) d\tau$ are both set to zero. Because the voltage v is either positive or negative for $t \in [mT, (m+(1/2))T]$ with $T = 2\pi/\omega$, $\phi(t)$ is strictly monotonically increasing or decreasing in the same time interval. Thus, $\phi = \phi(t)$ can be inverted for $t \in [mT, (m+(1/2))T]$, i.e., $t = g(\phi)$. $q(t)$ can then be reformulated as $q(t) = q(g(\phi)) = f(\phi)$, which indicates that q is a single-valued function of ϕ in the interval $[mT, (m+(1/2))T]$. Similarly, for $t \in [(m+(1/2))T, (m+1)T]$, we can prove that q is the same single-valued function of ϕ as well. All these demonstrate that (29) and (30) indeed characterize an ideal memristor.

IV. CONCLUSION

We reveal our physical analysis of memristance, memcapacitance, and meminductance. They are due to different combinations of linear and nonlinear electric responses. The pinched hysteresis loop is caused by the nonlinear responses of even number orders, i.e., $2k\omega$ nonlinear terms. The linear responses correspond to conventional resistance, capacitance, or inductance, and the nonlinear responses of odd number orders, i.e., $(2k+1)\omega$ terms, correspond to nonlinear resistance, nonlinear capacitance, or nonlinear inductance, respectively. The understanding of their physical origins may help search for and design novel memristors, memcapacitors, and meminductors.

REFERENCES

- [1] L. Chua, "Memristor and memristive systems symposium," Univ. California, Berkeley, CA, USA, 2008. [Online]. Available: <https://www.youtube.com/watch?v=QFdpZcZwbs>
- [2] L. Chua, "Introduction to memristors," IEEE, New York, NY, USA, 2009. [Online]. Available: <https://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=EDP091&contentType=Education+%26+Learning>
- [3] L. O. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.
- [4] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, no. 2, pp. 209–223, Feb. 1976.
- [5] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
- [6] R. Williams, "How we found the missing memristor," *IEEE Spectr.*, vol. 45, no. 12, pp. 28–35, Dec. 2008.
- [7] L. O. Chua, "Nonlinear circuit foundations for nanodevices. i. The four-element torus," *Proc. IEEE*, vol. 91, no. 11, pp. 1830–1859, Nov. 2003.
- [8] L. Chua, "Resistance switching memories are memristors," *Appl. Phys. A*, vol. 102, no. 4, pp. 765–783, Mar. 2011.
- [9] X. Zheng, Y. J. Yan, and M. Di Ventra, "Kondo memory in driven strongly correlated quantum dots," *Phys. Rev. Lett.*, vol. 111, no. 8, Aug. 2013, Art. ID. 086601.
- [10] K.-H. Kim *et al.*, "A functional hybrid memristor crossbar-array/cmos system for data storage and neuromorphic applications," *Nano Lett.*, vol. 12, no. 1, pp. 389–395, Dec. 2011.
- [11] S. P. Adhikari, M. P. Sah, K. Hyongsuk, and L. O. Chua, "Three fingerprints of memristor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 3008–3021, Nov. 2013.
- [12] L. Chua, "Memristor, hodgkin huxley, and edge of chaos," *Nanotechnology*, vol. 24, no. 38, Sep. 2013, Art. ID. 383001.
- [13] L. O. Chua, "The fourth element," *Proc. IEEE*, vol. 100, no. 6, pp. 1920–1927, Jun. 2012.
- [14] M. Di Ventra and Y. V. Pershin, "On the physical properties of memristive, memcapacitive and meminductive systems," *Nanotechnology*, vol. 24, no. 25, Jun. 2013, Art. ID. 255201.
- [15] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic memristor through spin-torque-induced magnetization motion," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 294–297, Mar. 2009.
- [16] J. J. Yang *et al.*, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature Nanotechnol.*, vol. 3, no. 7, pp. 429–433, Jul. 2008.
- [17] S. H. Jo *et al.*, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, 2010.
- [18] M. J. Lee *et al.*, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric ta2o5-x/tao2-x bilayer structures," *Nature Mater.*, vol. 10, no. 8, pp. 625–630, 2011.
- [19] J. J. Yang *et al.*, "The mechanism of electroforming of metal oxide memristive switches," *Nanotechnology*, vol. 20, no. 21, pp. 1–9, May 2009.
- [20] Y. Ho, G. Huang, and P. Li, "Dynamical properties and design analysis for nonvolatile memristor memories," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 4, pp. 724–736, Apr. 2011.
- [21] A. Ascoli, F. Corinto, V. Senger, and R. Tetzlaff, "Memristor model comparison," *IEEE Circuits Syst. Mag.*, vol. 13, no. 2, pp. 89–105, 2nd Quart. 2013.
- [22] D. Biolek, Z. Biolek, and V. Biolkova, "Pinched hysteretic loops of ideal memristors, memcapacitors and meminductors must be 'self-crossing,'" *Electron. Lett.*, vol. 47, no. 25, pp. 1385–1387, Dec. 2011.
- [23] Z. Biolek, D. Biolek, and V. Biolkova, "Computation of the area of memristor pinched hysteresis loop," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 9, pp. 607–611, Sep. 2012.
- [24] C. Sanchez-Lopez, J. Mendoza-Lopez, M. Carrasco-Aguilar, and C. Muniz-Montero, "A floating analog memristor emulator circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 309–313, May 2014.
- [25] D. Biolek, Z. Biolek, and V. Biolkova, "Interpreting area of pinched memristor hysteresis loop," *Electron. Lett.*, vol. 50, no. 2, pp. 74–75, Jan. 2014.
- [26] S. Kvatinisky, E. Friedman, A. Kolodny, and U. Weiser, "Team: Threshold adaptive memristor model," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 211–221, Jan. 2013.
- [27] J. Mason and D. Handscomb, *Chebyshev Polynomials*. Boca Raton, FL, USA: CRC Press, 2003.