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A multi-scale modeling of junctionless field-effect transistors

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In this work, we simulate a realistic junctionless (JL) field-effect transistor using a multi-scale approach. Our approach features a combination of the first-principles atomistic calculation, semi-classical semiconductor device simulation, compact model generation, and circuit simulation. The transfer characteristics of JL transistors are simulated by a recently developed quantum mechanical/electromagnetics method, and good agreement is obtained compared to experiment. A compact model for JL transistors is then generated for subsequent circuit simulation. We demonstrate a multi-scale modeling framework for quantum mechanical effects in nano-scale devices for next generation electronic design automation. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4817911]

Continuous miniaturization of semiconductor devices has reached the 22 nm node and is expected to approach the 10 nm node and beyond before 2026.[1] Atomic features and quantum mechanical (QM) effects in highly scaled devices have become more pronounced than ever before, and some are even exploited as functioning mechanism of a range of new devices, such as transistors based on quantum dots[2] and tunneling field-effect-transistors (TFET).[3] The presence of QM effects, due to the significantly enhanced physical complexity, has imposed substantial challenges on designing nano-electronic systems. An appropriate modeling of QM effects, maintaining balance between accuracy and efficiency across different design levels, is crucial to the success of electronic design automation (EDA) as well as nanoelectronics in the next decade.

First-principles calculation with atomistic structures provides the most accurate characterization of QM phenomena. The limited modeling capacity (tens of thousands of atoms), however, renders it not suitable to simulate an entire device. An effective approach to include QM effects is the multi-scale method,[4–6] where the important part of the device is modeled with atomistic details and the remaining parts plus the surrounding structures are treated by classical models for higher computational efficiency. The rationale behind is that the QM effects having major effects on device characteristics are confined to small regions (e.g., the channel and gate oxide); in the other parts (e.g., source/drain and substrate), the QM effects are less important and classical models will suffice for modeling purpose. One such multi-scale QM framework, which integrates an atomistic QM simulator and a semi-classical electromagnetic-drift-diffusion solver (called the QM/EM (electromagnetic) method), has been reported in Refs. 4 and 5, where good agreement with full QM simulation has been demonstrated.

Recently, junctionless (JL) silicon nanowire (SiNW) field-effect transistors were fabricated with no pn junction and thereby eliminating the doping concentration gradient.[7] This avoids the difficulty to fabricate the ultrashallow junctions. With a tri-gate structure, JL transistors provide better gating control and are found to have superior subthreshold slope and low leakage voltage. Theoretical studies also find JL transistors have better subthreshold behavior than classical inversion mode transistors.[8] In this letter, we report a multi-scale modeling of the JL transistors. By applying the QM/EM method, the transfer characteristics of a realistic JL transistor is simulated. Based on the QM/EM simulations, a compact model is constructed and then incorporated into a circuit simulator to simulate a simple circuit constructed from JL transistors. In the current approach, the term "multi-scale" refers not only to physical scale but also to abstraction level, which represents an integrated flow spanning from atomistic QM calculation, technology computer-aided-design (TCAD) simulation, and compact model generation to circuit simulation.

We use the non-equilibrium Green's function (NEGF) formalism[9,10] for simulations of quantum transport properties of nano-devices. The device under study is connected to two semi-infinite leads characterized by self-energies. In this work, a density functional tight-binding (DFTB)[11] description of the system is adopted. The Hamiltonian and overlap matrix elements are numerically pre-calculated using *ab initio* density functional theory (DFT). To solve the transport problem, the contacting leads are assumed to be in equilibrium at different chemical potential, driving the device out of equilibrium. The density matrix can be computed as

$$\rho = -\frac{i}{2\pi}\int_{\infty}^{\infty} G^{<}(E)dE, \tag{1}$$

where $G^{<}$ is the lesser Green's function, giving the spectral density of occupied states. It is expressed as

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$$G^<(E) = G^r(E)\Sigma^<(E)G^{r\dagger}(E),$$
$$G^r(E) = [ES - H + \Sigma^r(E)]^{-1}, \quad (2)$$

where G^r is the retarded Green's functions. $\Sigma^<, \Sigma^r$ are the lesser and retarded self-energies, respectively. S is the overlap matrix. In DFTB, the Hamiltonian H is given by

$$H_{\mu\nu} = H^0_{\mu\nu} + \frac{1}{2}(\delta V_\mu + \delta V_\nu)S_{\mu\nu}, \quad (3)$$

where the first term is the zero-order DFTB Hamiltonian, while the second term contains Hartree potential and exchange-correlation potential due to change of electron density. Poisson equation is solved

$$\nabla^2\phi(\mathbf{r}) = 4\pi n(\mathbf{r}), \quad (4)$$

where $\phi(\mathbf{r})$ and $n(\mathbf{r})$ are real space potential and electron density distribution, respectively, and δV is obtained by projecting $\phi(\mathbf{r})$ on the atomic sites.[12] The retarded self-energy function in Eq. (2) is given by

$$\Sigma^r(E) = (ES - h)^\dagger g^r(E)(ES - h), \quad (5)$$

where h is the coupling matrix between the leads and device. g^r is the surface Green's function of leads. The leads are assumed to be semi-infinite periodic lattice and can be evaluated by standard renormalization method.[13] To increase the efficiency, a recently developed method[14] is employed, where a condensed contact Hamiltonian can be exploited to construct the surface Green's function. The lesser self-energy represents the injection of charge from the leads and can be written in terms of retarded self-energy

$$\Sigma^<(E) = -2if(E)\mathrm{Im}[\Sigma^r(E)], \quad (6)$$

where f is the Fermi function.

Equations (1) and (4) are then solved self-consistently, and the current flowing through the electronic device can be evaluated via the Landauer formula[15,16]

$$I(V) = \frac{2e^2}{h}\int_{-\infty}^{\infty} T(E,V)[f^L(E) - f^R(E)]dE, \quad (7)$$

where $T(E,V)$ is the transmission coefficient at energy E under bias voltage V. The transmission coefficient is related to Green's functions by

$$T(E,V) = \mathrm{Tr}[\Gamma_L(E)G^r(E,V)\Gamma_R(E)G^a(E,V)], \quad (8)$$

where $\Gamma(E)$ is the coupling at energy E between the device and the leads.

The DFTB method allows an efficient construction of Hamiltonian. The combination with the recursive Green's function algorithm,[17] and the fast evaluation of self-energies[14] enables a first-principles treatment of more than 50 000 atoms on a dual Xeon E5620 workstation.

Simulation of entire semiconductor devices is generally inaccessible by atomistic QM methods. To simulate realistic electronic devices, a recently developed hybrid QM/EM method[4,5] is used in which the system is partitioned into QM regions which are described by quantum mechanics, and EM regions where classical models are used. Typical QM regions include the conducting channel while EM regions comprise of interconnects and semiconductor substrate. An illustration of the QM/EM partition of an electronic device is shown in Fig. 1(a).

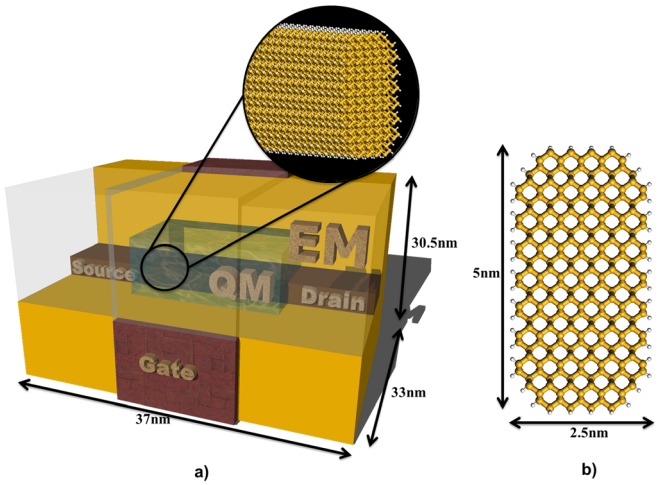

FIG. 1. (a) An illustration of the QM and EM domains. The QM domain (inner box) contains the SiNW and is simulated by QM transport model with full atomistic details and the remaining EM domain, comprising gate dielectric, source/drain, is treated classically. (b) Cross section of a 25 nm long SiNW JL transistor.

In this work, the quantum transport of the conducting channel is solved using DFTB+NEGF method, and its electromagnetic environment is provided by the EM simulator. In the EM simulator, carriers in semiconductor are described by the drift-diffusion (DD) model, and a coupled EM and classical-charge-dynamics approach based on the finite volume method (FVM) is adopted,[18,19] where the DD equations

$$\vec{J} = q\mu n\vec{E} + kT\mu\nabla n \quad (9)$$

are coupled with the Maxwell's equations and solved using Newton's method. Concerning the small size of the transistor in this work and only steady state properties are simulated, the effect of magnetic field is neglected, and only Poisson equation is solved. In cases when magnetic field effects become important, both scalar and vector potential have to be included, and Maxwell's equations have to be solved.[5] It is also noted that more advanced TCAD models for semiconductor devices can be readily used to replace the DD model for more sophisticated description in the non-QM regions.

Information exchange between QM and EM models plays a key role in the QM/EM method. The two models are solved in a self-consistent manner and coupled via boundary conditions at the interfaces of the QM and EM regions. At first step, the classical EM model is solved to obtain the potential distribution for the whole simulation domain. The potential at the interfaces is identified and used as boundary condition for the QM model. Quantum transport equations are solved, and current passing through the channel is obtained from Eq. (7). The current density is then used as boundary condition, satisfying the current continuity at the interfaces in the next EM calculation. This process is iterated until the current and potential at the interface converge.

The experimental realization of JL SiNW field-effect transistors[7] potentially alleviates the increasingly difficult fabrication challenge in the semiconductor industry. The smallest JL transistor reported has a diameter down to 4 nm.[20] In this work, we apply the QM/EM method to simulate JL transistors with dimensions comparable to experiments. The structure of the JL transistor in our simulations is shown in Fig. 1. The entire device is divided into the QM and EM regions. The QM region contains an atomistic SiNW as the conducting channel, while the gate dielectric, gate, source, and drain electrodes constitute the EM region. As shown in Fig. 1(a), the device has a gate-all-around (GAA) architecture. We consider a [110]-oriented SiNWs, the most common growth orientation for wires below 10 nm.[21] A hydrogen-terminated surface is adopted to model SiNW. The SiNW is 25 nm long with a 5 nm by 2.5 nm cross section, giving rise to a total of 15616 atoms in the QM region. To model doped SiNWs, Si atoms are substituted by As atoms for *n*-type doping and Ga atoms for *p*-type doping. We evenly distribute 4 dopants in the channel which corresponds to 1.3×10^{19} cm^{-3} doping concentration for a 20 nm long channel. The QM region is enclosed in an EM region with a dimension of $37 \times 33 \times 30.5$ nm^3, comprising gate dielectric, source, and drain electrodes. Following Ref. 20, a 14 nm thick effective gate oxide and 20 nm gate length are adopted in the EM region. Silicon dioxide is used for the gate dielectric, and *n*-doped silicon is used for source and drain. The dielectric constants for silicon dioxide and silicon are 3.9 and 11.9, respectively.[22] The mobility is 0.045 and $0.15\,m^2V^{-1}s^{-1}$ for holes and electrons, respectively. Dirichlet boundary condition is applied to the contact region while Neumann boundary condition is applied to remaining part on the EM domain. A 50 mV drain bias and various gate voltage are applied to obtain the transfer characteristics. The EM domain provides the electrostatic environment for SiNW JL transistor where the quantum transport equations are solved. Temperature 300 K is used throughout the simulations.

Fig. 2 plots the $I - V_G$ characteristics for *n*-type JL transistor. The green curve represents the simulation result from QM/EM method. Giving the same ON/OFF ratio, the result shows that good agreement is obtained between our simulations and experiment.[20] To further verify the QM/EM simulation results, we simulate the same JL structure with the 3D commercial TCAD simulator Silvaco Atlas using the built-in NEGF mode-space (NEGF_MS) solver to model the quantum effects.[23] The drain currents of the two simulators are compared in Fig. 2. It can be seen that QM/EM results agree well with Atlas in the subthreshold region, indicating that the quantum confinement and source-to-drain tunneling are accurately captured. The non-monotonic behavior in the transconductance of QM/EM simulation results can be explained by the lack of phonon scattering in our NEGF formulation and the corresponding neglect of energy level broadening. This leads to abrupt change in the conduction current when energy levels fall into/out of the bias window. Inspection of the local density of state (LDOS) Figs. 2(b) and 2(c) shows that peaks at ±5 nm (correspond to the dopant positions) are pushed out of the bias window when the gate voltage is increased from −0.7 V to −0.9 V. This leads to a rapid drop of conduction current. We note that similar

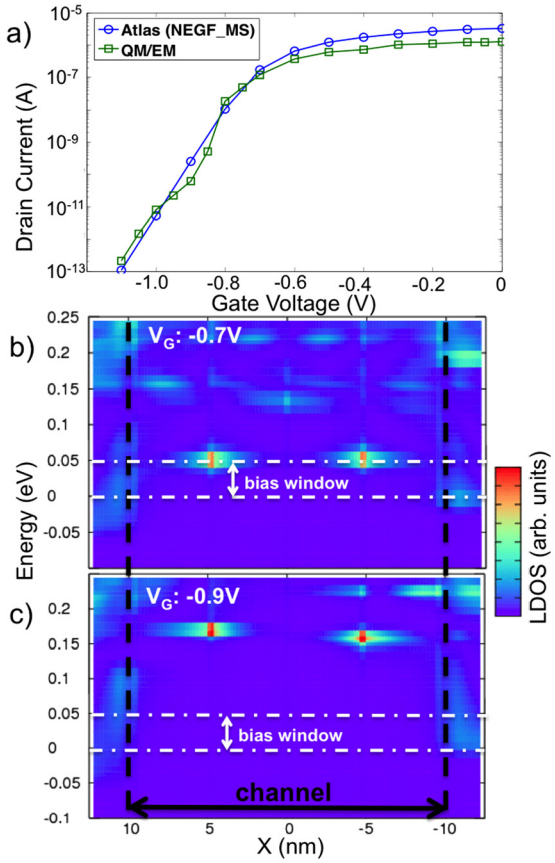

FIG. 2. Drain current versus V_G for *n*-type SiNW JL transistor doped by As atoms with dimensions shown in Fig. 1. Blue line: simulation results of Atlas and green line: simulation results of QM/EM method. Local density of state of the JL transistor with gate voltage (b) −0.7 V and (c) −0.9 V. Black dashed lines indicate the channel region, and white dashed lines indicate the bias window.

non-monotonous behaviour in the transfer characteristics of MOSFETs with confined Si channels has been demonstrated very recently in low temperature measurements that also lack level-broadening of the energy spectrum.[24,25] Both simulations show that the JL transistor has good electrostatic control and subthreshold characteristic. It is noted that the current from Atlas simulation is larger than that from QM/EM simulation in the linear region (the ON state), by around 2.5× at the flatband voltage. Assuming a homogeneous doping concentration in the conducting channel, the NEGF model in Atlas does not include impurity scattering due to dopants and is expected to give an upper limit of the current. In reality, impurity scattering can largely reduce the mobility in JL transistors, resulting in lower ON currents.

Compact modeling is an important vehicle for information transfer from technology fabrication to circuit and product design.[26] We extend the recently-developed compact model for tri-gate JL transistors[27] to model the GAA JL transistors. The strength of the model lies in its strong physics-based nature, so only 3 fitting parameters (A_1, A_3, and v_{sat}) are needed to be determined by simulation or measurement data. It also includes appropriate models for a range of physical effects specific to JL transistors, such as temperature-dependence of incomplete ionization, quantum confinement effects, and short channel effects. The model has been compared against measurement data, and good agreements have

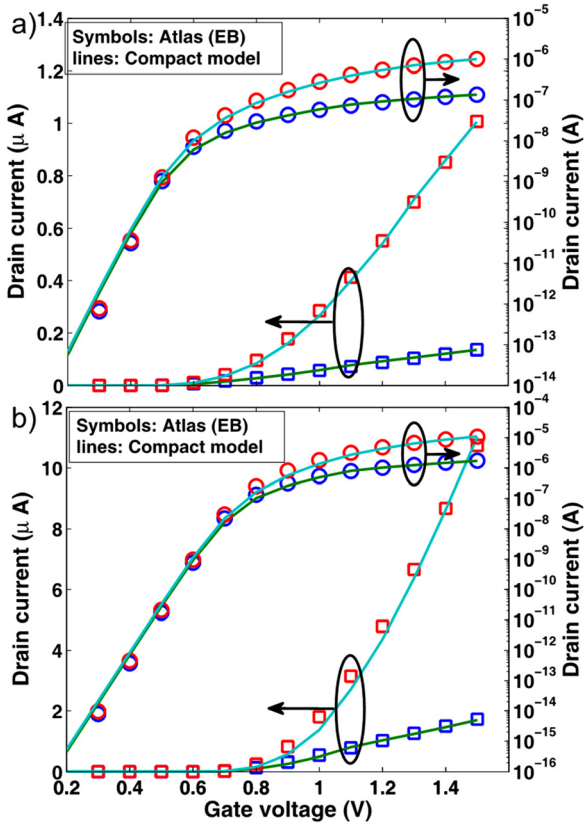

FIG. 3. Drain currents comparisons between Atlas and compact model for JL transistors of $10 \times 10\,\text{nm}^2$ cross-section, n-type of $1 \times 10^{19}\,\text{cm}^{-3}$. (a) 1 μm length, 4 nm oxide thickness, (b) 100 nm length, 2 nm oxide thickness. Both linear and log scales comparisons are shown.

been demonstrated. For more technical details we refer the readers to the original work.[27]

The model is adapted in the current work to treat GAA architecture. To verify the accuracy of the developed compact model, 3D TCAD simulation of n-type devices with two different geometries are performed with Silvaco Atlas using a semi-classical (energy balance (EB)) model.[23] The drain currents from Atlas and the compact model are compared in Fig. 3. Note that the same set of fitting parameters ($A_1 = 12, A_3 = 3, v_{sat} = 10^7\,\text{cm/s}$) are used in the compact model. As it can be seen, the compact model provides an accurate prediction of the drain current.

We then fit the compact model from the QM/EM simulation data. A_1 is tuned to fit the QM/EM simulation results.

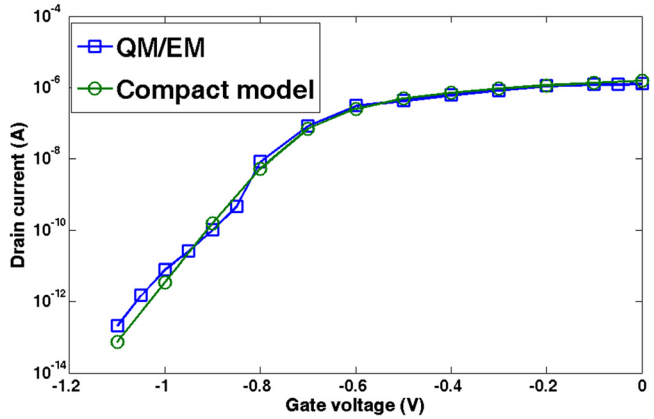

FIG. 4. Drain current versus V_G for n-type SiNW JL transistor. Blue line: simulation results of QM/EM method and green line: compact model.

All other fitting parameters in the compact model take the same values as the ones used in Fig. 3. The drain current predicted by the resultant compact model is compared in Fig. 4, where a reasonable agreement is observed. Since the quantum confinement has been taken into account, the compact model provides a good description of the device behavior in the subthreshold region.

The generated compact model is incorporated into a SPICE-like simulator SMORES[28] to simulate an inverter circuit consisting of one n-type and one p-type JL transistors, as shown in Fig. 5(a). Fig. 5(b) plots the transient response of the circuit. Since the time scale in the circuit simulation is on the order of nanosecond while the electron response in the transistor is on the order of femtosecond. The transistor is assumed to response instantaneously to the transient applied voltage. It is shown that the output waveform is correctly "inverted" from the input voltage which confirms the functionality of the compact model. With the high ON/OFF ratio and good subthreshold characteristics of the JL transistors, the inverter features a high peak-valley voltage difference.

We have shown that the QM/EM method is capable to calculate efficiently the I-V characteristics of a realistic JL transistor. The method features a full atomistic QM treatment of electronic devices where quantum effects like impurity scattering, quantum confinement,[29] dopant deactivation[30] are captured. Also, the interaction with electrostatic environment is taken into account self-consistently. From the calculated I-V curves, the compact model for the JL transistors is

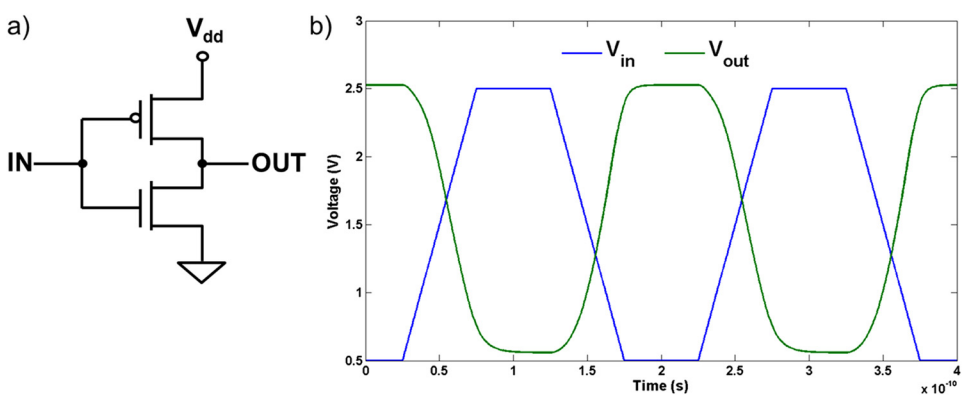

FIG. 5. (a) Circuit diagram of inverter. (b) Simulated I/O voltages of the inverter characterized by the generated compact model. Blue line: input voltage and green line: output voltage.

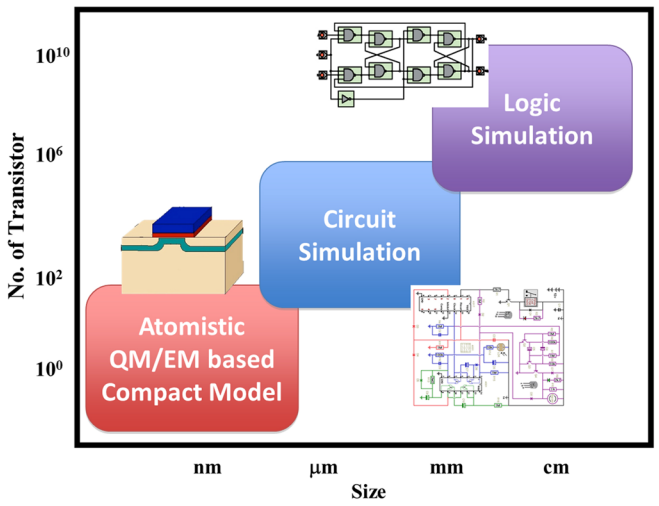

FIG. 6. Multi-scale approach in next generation EDA tool. The approach spans from atomistic calculations to hardware design.

constructed and employed to simulate the dynamics of an inverter made of the two JL transistors. Based on the modeling and simulation of the JL transistors and their circuits, we propose a multi-scale framework for next generation EDA tool as illustrated in Fig. 6. It starts from the most fundamental first-principles quantum mechanics characterization of nanoscale structures, goes all the way up to the classical modeling of semiconductor devices and compact modeling generation for large-scale circuit simulation. The success of this framework could enable the first-principles accuracy to come into the chip-level simulation and the engineers' world, but requires an extension of the physical basis underlying compact models, that would capture quantum effects beyond the electrostatic implication of channel quantisation. In the longer term, the seamless connection between the atomistic first-principles quantum mechanical calculation and the circuit simulation can be further enhanced by the rapid development of computational power and numerical algorithms.

We have presented the development of simulation tools with the aim of providing the atomistic level of understanding capability for circuit design and with the hope that these tools will help us to design new devices and circuits. Application to the simulation of JL transistor has demonstrated in principle the viability of this EDA flow, starting from atomistic QM simulation all the way to integrated circuit design, and hardware logic design.

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[1]*International Technology Roadmap for Semiconductors: Executive Summary* (2011).
[2]M.-H. Devoret and R.-J. Schoelkopf, Nature **406**, 1039–1046 (2000).
[3]A. M. Ionescu and H. Riel, Nature **479**, 329–337 (2011).
[4]C. Y. Yam, L. Meng, G. H. Chen, Q. Chen, and N. Wong, Phys. Chem. Chem. Phys. **13**, 14365–14369 (2011).
[5]L. Meng, C. Y. Yam, S. Koo, Q. Chen, N. Wong, and G. H. Chen, J. Chem. Theory Comput. **8**, 1190–1199 (2012).
[6]M. A. der Maur, G. Penazzi, G. Romano, F. Sacconi, A. Pecchia, and A. Di Carlo, IEEE Trans. Electron Devices **58**, 1425–1432 (2011).
[7]J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nat. Nanotechnol. **5**, 225–229 (2010).
[8]J. Z. Huang, W. C. Chew, J. Peng, C. Y. Yam, L. J. Jiang, and G. H. Chen, IEEE Trans. Electron Devices **60**, 2111–2119 (2013).
[9]L. Keldysh, Sov. Phys. JETP **20**, 1018 (1965).
[10]S. Datta, *Electronic Transport in Mesoscopic System* (Cambridge University Press, 1995).
[11]M. Elstner, D. Porezag, G. Jungnickel, J. Elsner, M. Haugk, T. Frauenheim, S. Suhai, and G. Seifert, Phys. Rev. B **58**, 7260–7268 (1998).
[12]A. Pecchia, G. Penazzi, L. Salvucci, and A. di Carlo, New J. Phys. **10**, 065022 (2008).
[13]M. P. L. Sancho, J. M. L. Sancho, and J. Rubio, J. Phys. F: Met. Phys. **15**, 851–858 (1985).
[14]J. Z. Huang, W. C. Chew, Y. Wu, and L. J. Jiang, J. Appl. Phys. **112**, 013711 (2012).
[15]R. Landauer, IBM J. Res. Dev. **1**, 223 (1957).
[16]M. Büttiker, Phys. Rev. Lett. **57**, 1761–1764 (1986).
[17]R. Lake, G. Klimeck, R. Bowen, and D. Jovanovic, J. Appl. Phys. **81**, 7845–7869 (1997).
[18]P. Meuris, W. Schoenmaker, and W. Magnus, IEEE Trans. Comput.-Aided Des. **20**, 753–762 (2001).
[19]W. Schoenmaker and P. Meuris, IEEE Trans. Comput.-Aided. Des. **21**, 534–543 (2002).
[20]S.-J. Choi, D.-I. Moon, J. P. Duarte, S. Kim, and Y.-K. Choi, in *Proceedings of VLSIT* (2011), pp. 74–75.
[21]Y. Wu, Y. Cui, L. Huynh, C. Barrelet, D. Bell, and C. Lieber, Nano Lett. **4**, 433–436 (2004).
[22]W. M. Haynes, *CRC Handbook of Chemistry and Physics*, 91st ed. (CRC Press, 2010).
[23]*Atlas User's Manual* (Silvaco Int., Santa Clara, CA 2012).
[24]S. Migita, Y. Morita, M. Masahara, and H. Ota, "Electrical performances of junctionless-FETs at the scaling limit (LCH = 3 nm)," Electron Devices Meeting (IEDM), 2012 IEEE International, pp. 8.6.1-8.6.4.
[25]X. Li, W. Han, L. Ma, H. Wang, Y. Zhang, and F. Yang, IEEE Electron Device Lett. **34**, 581 (2013).
[26]Semiconductor Research Corporation (SRC), "Research needs for compact modeling," Technical Report, 2013.
[27]R. Trevisoli, R. Doria, M. De Souza, S. Das, I. Ferain, and M. Pavanello, IEEE Trans. Electron Devices **59**, 3510–3518 (2012).
[28]B. N. Bond, SMORES: A Matlab tool for simulation and model order reduction of electrical systems, 2010.
[29]G. Bryant, Phys. Rev. B **29**, 6632–6639 (1984).
[30]M. Björk, H. Schmid, J. Knoch, H. Riel, and W. Riess, Nat. Nanotechnol. **4**, 103–107 (2009).