A Multi-Scale Framework for Nano-electronic Devices Modeling with Application to the Junctionless Transistor

Jie Peng*, Quan Chen†, Ngai Wong†, LingYi Meng*, ChiYung Yam* and GuanHua Chen*
*Department of Chemistry, The University of Hong Kong, Hong Kong
Email: kitpeng@hku.hk, lymeng@yangtze.hku.hk, yamcy@yangtze.hku.hk and ghc@yangtze.hku.hk
†Department of Electrical and Electronic Engineering, the University of Hong Kong
Email: quanchen@eee.hku.hk and nwong@eee.hku.hk

***Abstract*—In this paper we present a new multi-scale simulation scheme for next-generation electronic design automation (EDA) for nano-electronics. The scheme features a combination of the first-principles quantum mechanical calculation, semi-classical semiconductor device simulation, compact model generation and circuit simulation. To demonstrate the feasibility of the proposed scheme, we apply our newly developed quantum mechanics/electromagnetics method to simulate the junctionless (JL) transistors. Based on the calculated I-V curves, a compact model is then constructed for the JL transistors. The validity of the compact model is further verified by the transient circuit simulation of an inverter.**

I. Introduction

The continuous miniaturization of semiconductor devices has reached the 22nm node and is expected to approach 10nm and beyond before 2026 [1]. Atomic features and quantum effects have become more pronounced than ever before, and some are even exploited as functioning mechanism of a range of new devices, such as transistors based on quantum dots [2] and wires [3] . The major challenges of the existing electronic design automation (EDA) tools are in how to incorporate the quantum phenomena into the classical semiconductor device models based on the continuum assumption. Full atomistic quantum mechanical (QM) calculation, while providing us with reliable characterizations of nano-scale systems, confronts severe applicability limitation due to the prohibitive computational cost. One natural workaround is the multi-scale method, where only a small portion of the device is characterized with QM description and the remaining (non-critical) parts of the device plus the surrounding structures are treated classically. The rationale behind lies in that the QM effects that have substantial influence on device properties are confined to a small region, outside which (e.g., in the bulk material) classical models suffice to provide reasonable characterizations. One such multi-scale method, which combines combines a first-principles QM simulator and a semi-classical electromagnetic-drift-diffusion solver (called the QM/EM method), has been reported [4], [5]. The QM/EM method has been applied to simulate the carbon nanotubes embedded in silicon substrates, and the good agreements with full QM simulation have been demonstrated.

Physics-based simulation of individual devices comprises only one part in the modern EDA flow. One level upward the technology hierarchy, compact modeling is another necessity to enable computer simulation of circuits involving millions of devices. Industry-standard compact models, such as the BSIM family, require fitting a large ensemble of measurement data usually costly to obtain, particularly for emerging devices where experiments may not be available or mature enough to provide reliable data.

The objective of this paper is to report a multi-scale flow for next-generation EDA tools that spans from the first-principles QM simulation to the generation of the compact models for circuit simulations. To demonstrate the feasibility of the entire flow, we apply the QM/EM method to the simulation of a new type of semiconductor device, the JL transistor, and generate a compact model based on the QM/EM results, which is then put into a circuit simulator to simulate a simple integrate circuit made of the JL transistors.

II. QM/EM Simulation

A. Basic Framework

The QM/EM method starts with partitioning the system of interest into QM regions which are described by quantum mechanics, and EM regions where classical models will be used. Typical domains that should be treated at QM level in a nanotransistor include the channel and parts of the source and drain for conduction currents. We did an external QM calculation with the gate included to demostrate the quantum depletion effect caused by the hetero-doped gate. The EM regions consist the remaining parts of the system.

The QM part of the system is solved by using our first-principles simulator *LODESTAR* [7], with the density-functional tight-binding (DFTB) method combined with the non-equilibrium Green's function (NEGF) method [8]. The EM solver combines the Maxwell's equations and the drift-diffusion (DD) model, as described in references [9], [10]. More advanced technology computer-aided design (TCAD) models for semiconductor devices can be readily used to replace the DD model for higher modeling requirements.

The two solvers are coupled via boundary conditions at the interfaces of the QM and EM regions. The EM solver is first applied in the whole domain to obtain an initial potential distribution. The potentials at the QM/EM interface then act as the boundary conditions for the QM calculation. In return, the current density through the QM/EM interface calculated by the QM solver is served as a part of the boundary conditions for the EM solver. The process is iterated until the current and potential at the interface converge. For more details we refer the readers to our previous papers [4], [5].

B. Application to Junctionless Transistor

In this section, we apply the QM/EM method to simulate a new type of semiconductor device, JL transistor. The structure of the JL transistor is shown in Fig. 1. The QM/EM region is divided differently in the ground state and steady state calculation. The QM region for ground state calculation includes a 6nm-long silicon nanowire doped by 6 Ga/As atoms along the (110) direction, which includes the source, channel and drain, and a "Π" shaped hetero/homo-doped gate (the gate doped with the same/different type of dopants). When the QM/EM method is applied to the more time consuming steady

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state calculation, the QM region is further cutted down to a 3 nm long silicon nanowire, as shown in Fig. 1, the blue region. The EM region consists the remaining parts of the structure in the EM box with the size of $8 \times 6 \times 6\ nm^3$, which is very difficult to be handled as a whole by existing atomistic QM simulators.

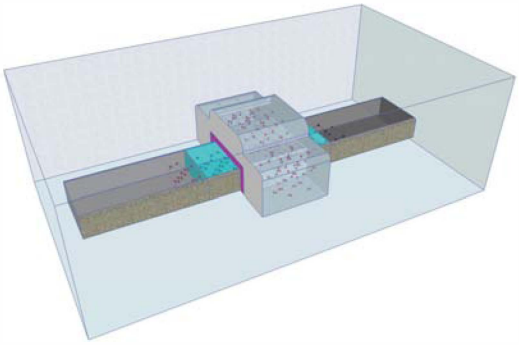

Fig. 1. The schematic representation of the QM/EM structure.

III. Compact Modeling

Parameter extraction is the essential part of compact modeling for semiconductor devices. The ultimate objective of our method is to replace the experimental data required in the parameter extraction process by the QM/EM simulation results. A direct connection between first-principles simulation and SPICE-compatible compact models helps to minimize costly experiment measurements and facilitate the modeling of emerging semiconductor devices from first-principles.

To demonstrate the multi-scale QM/EM-to-SPICE modeling process, we generate a primitive compact model for JL transistor using the I-V curves obtained by the QM/EM simulation. Our compact model formulation is based upon a recently developed model [12] for the JL transistors. The drain-to-source currents I_{ds} are modeled separately in the subthreshold, linear and saturation regions. Several modifications are made to the original model [12] to render it suitable for our problem.

The $I - V_{gate}$ curves from the compact model are shown in Fig. 2. In addition, we incorporate the generated compact model into a Matlab-based SPICE-like simulator SMORES [13] to simulate an inverter circuit consisting of two JL transistors, as shown in Fig. 3 (a). The transient response is shown in Fig. 3 (b). The output waveform is generally "inverted" from the input waveform, which verifies the functionality of the inverter.

IV. Conclusion

We have presented the development of a new generation of simulation tools with the aim of providing the atomistic level of understanding capability for circuit design and with the hope that these tools may help us to design new devices and circuits. Application to the simulation of JL transistor has demonstrated in principle the viability of the new EDA flow. The EDA tool starting from atomistic QM simulation all the way to integrated circuit design of sub-16nm may thus be possible.

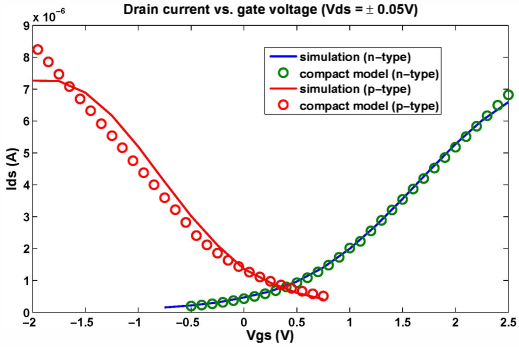

Fig. 2. $I - V_{gate}$ curves from QM/EM simulation and compact modeling.

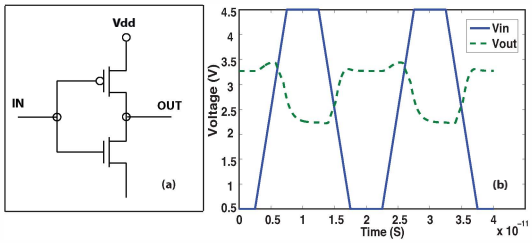

Fig. 3. (a) Circuit diagram of inverter. (b) Simulated I/O voltages with the generated compact model.

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